ABSTRACT OF THE DISCLOSURE

A speculative branch target address cache (BTAC) in a microprocessor. The BTAC caches target addresses and other information about branch instructions, such as instruction length, location within an instruction cache line, and a direction prediction. The BTAC is indexed by a fetch address of the microprocessor's instruction cache to determine whether a BTAC hit occurs. The BTAC is accessed early in the pipeline in parallel with the instruction cache access prior to decoding any instructions in the indexed instruction cache line. If a hit occurs in the BTAC, and the BTAC direction prediction is taken, the microprocessor speculatively branches to the target address supplied by the BTAC. The branch is speculative because the instructions in the cache line have not yet been decoded; hence, there is no guarantee that the alleged branch instruction associated with the information cached in the BTAC is present in the instruction cache.